

1/7

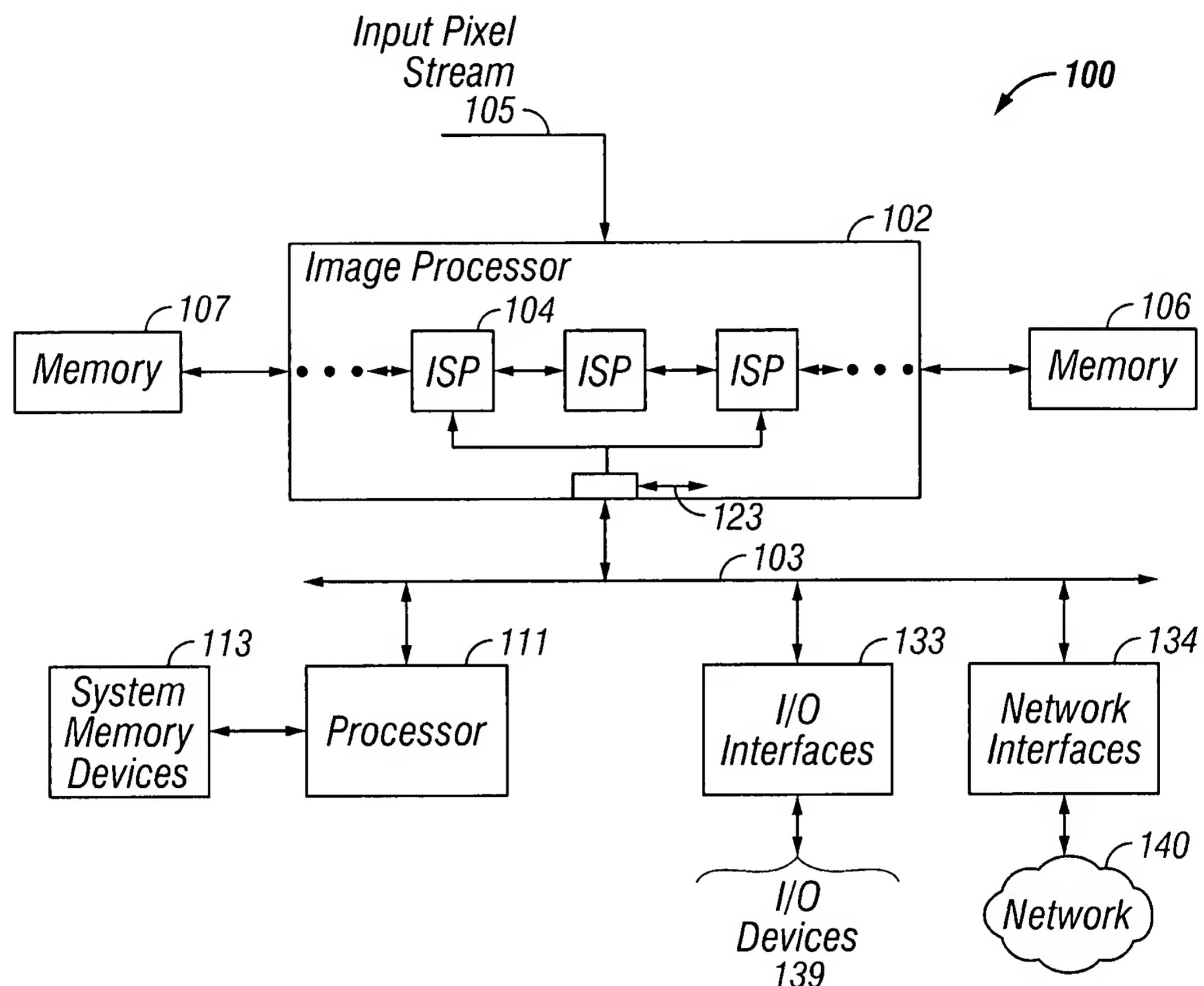


FIG. 1

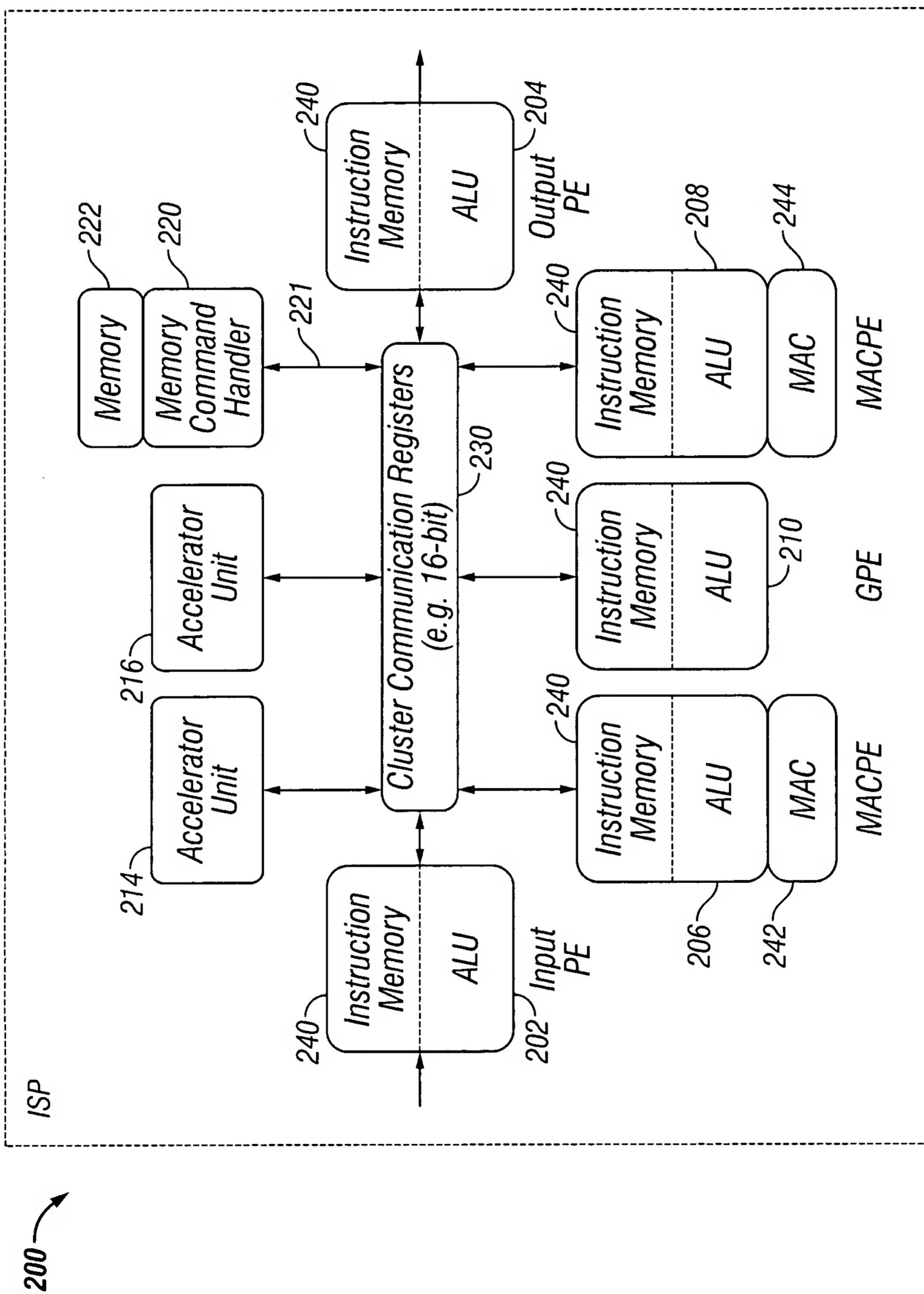


FIG. 2

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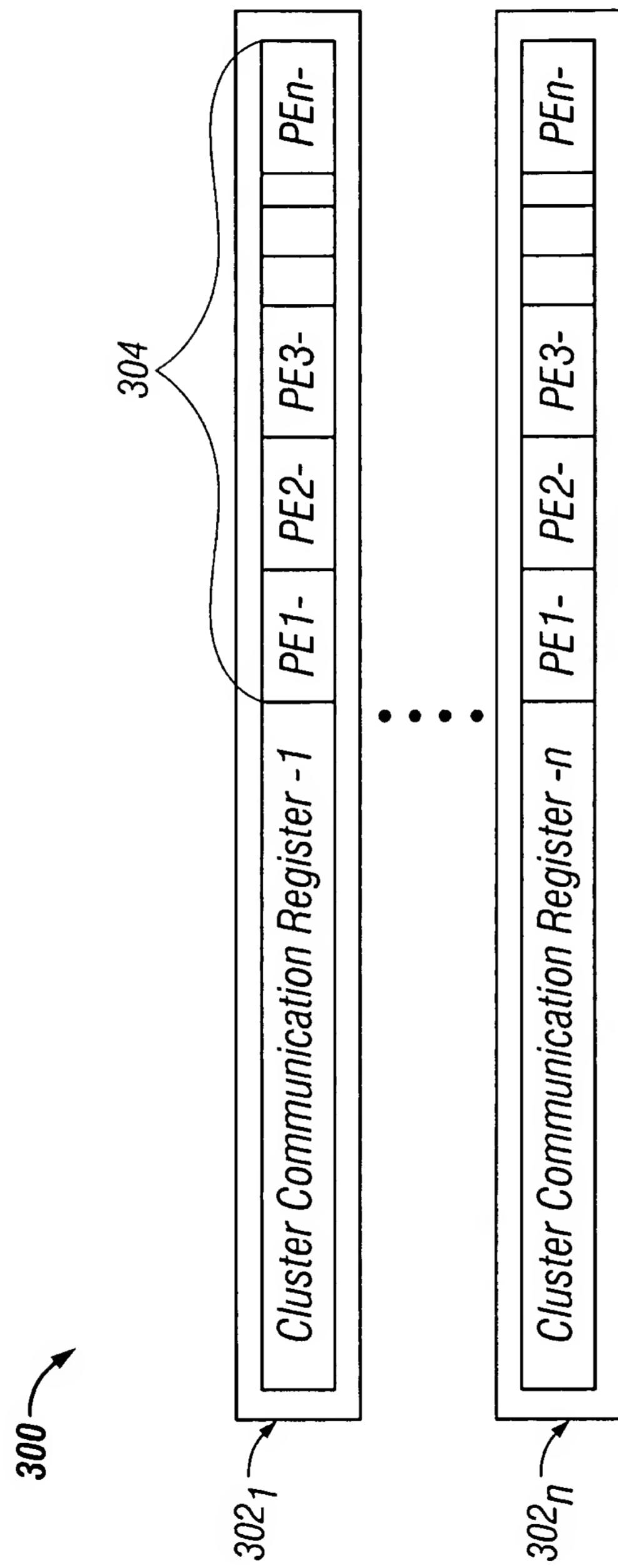


FIG. 3

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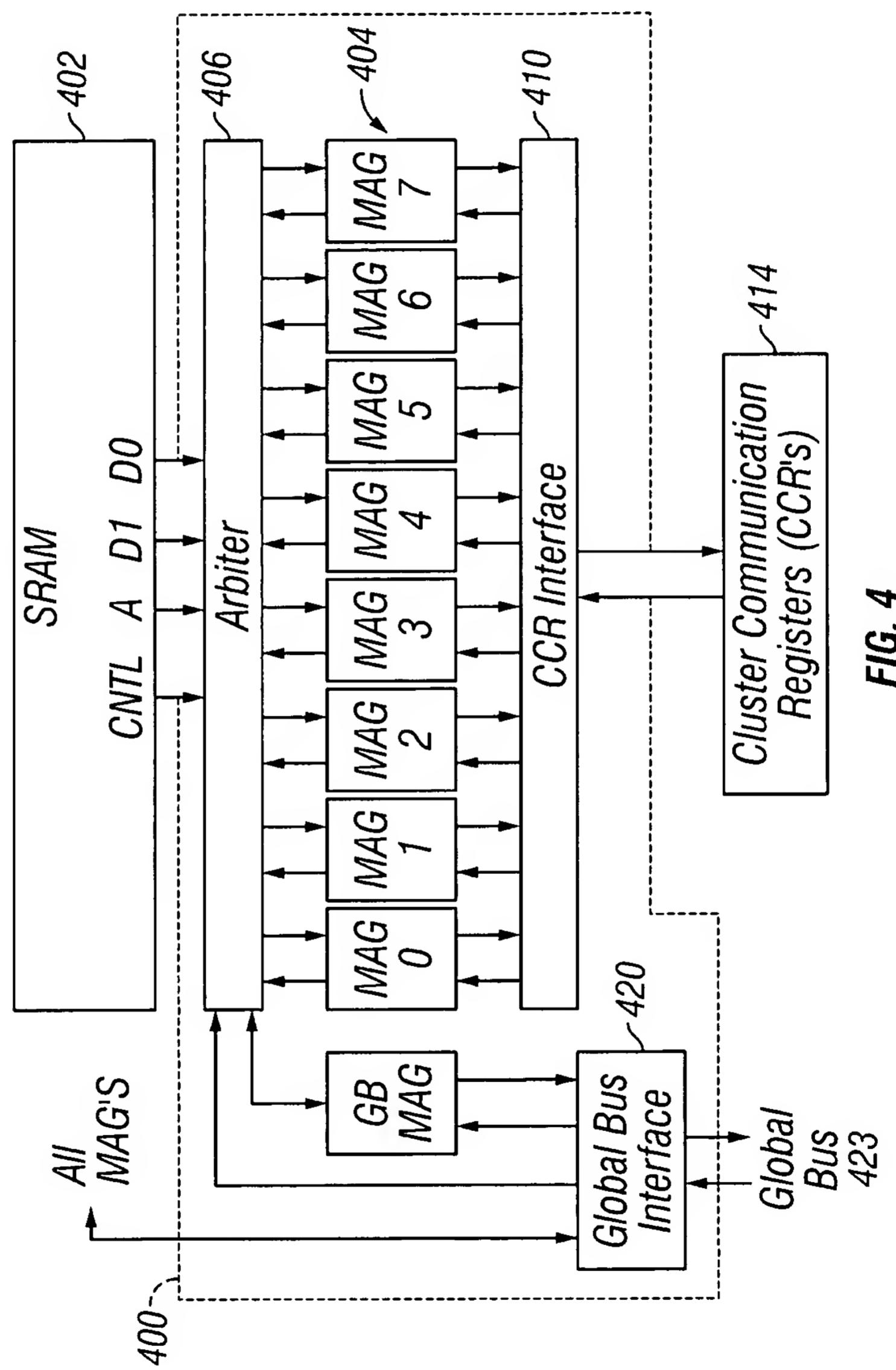


FIG. 4

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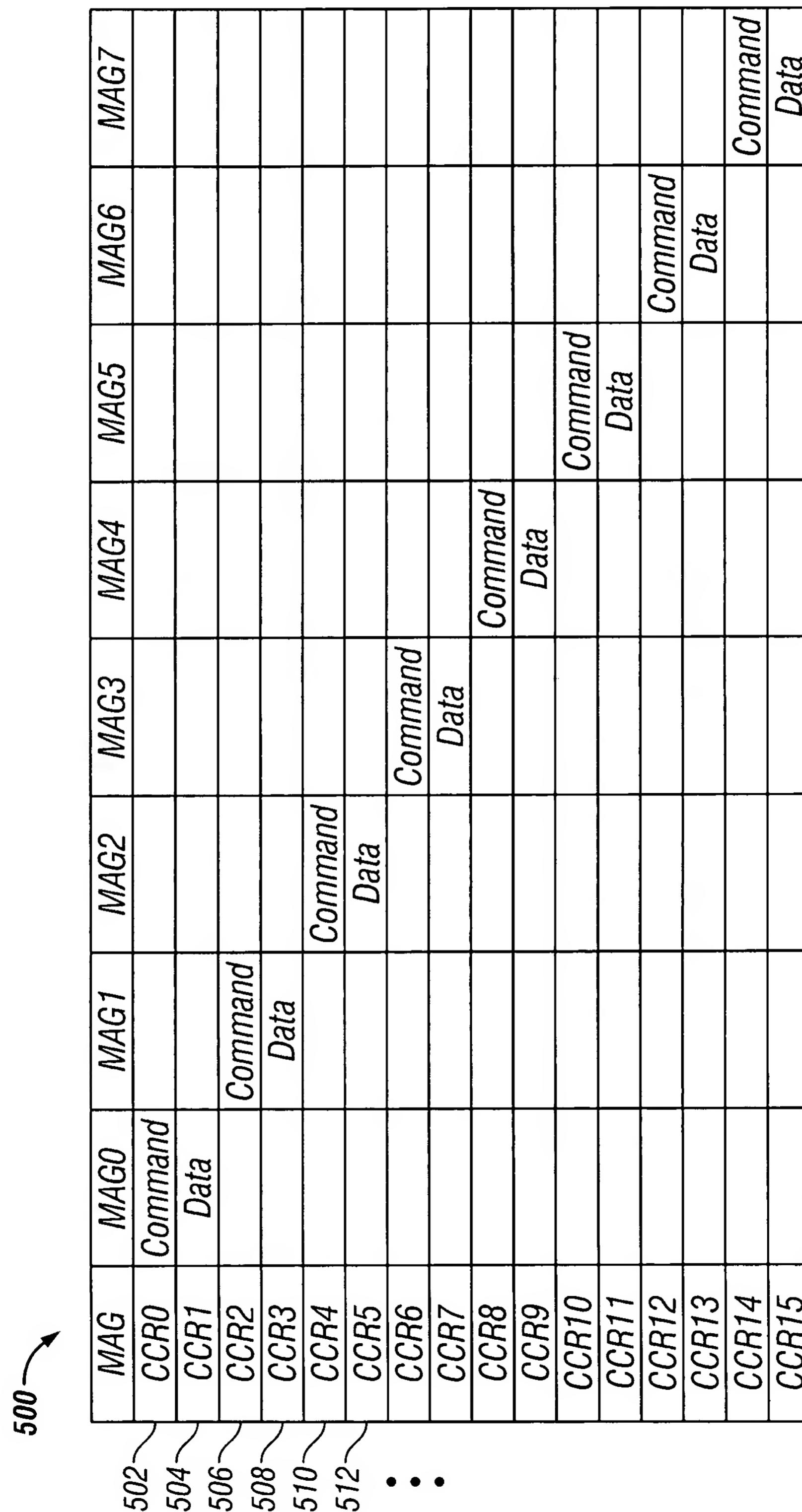


FIG. 5

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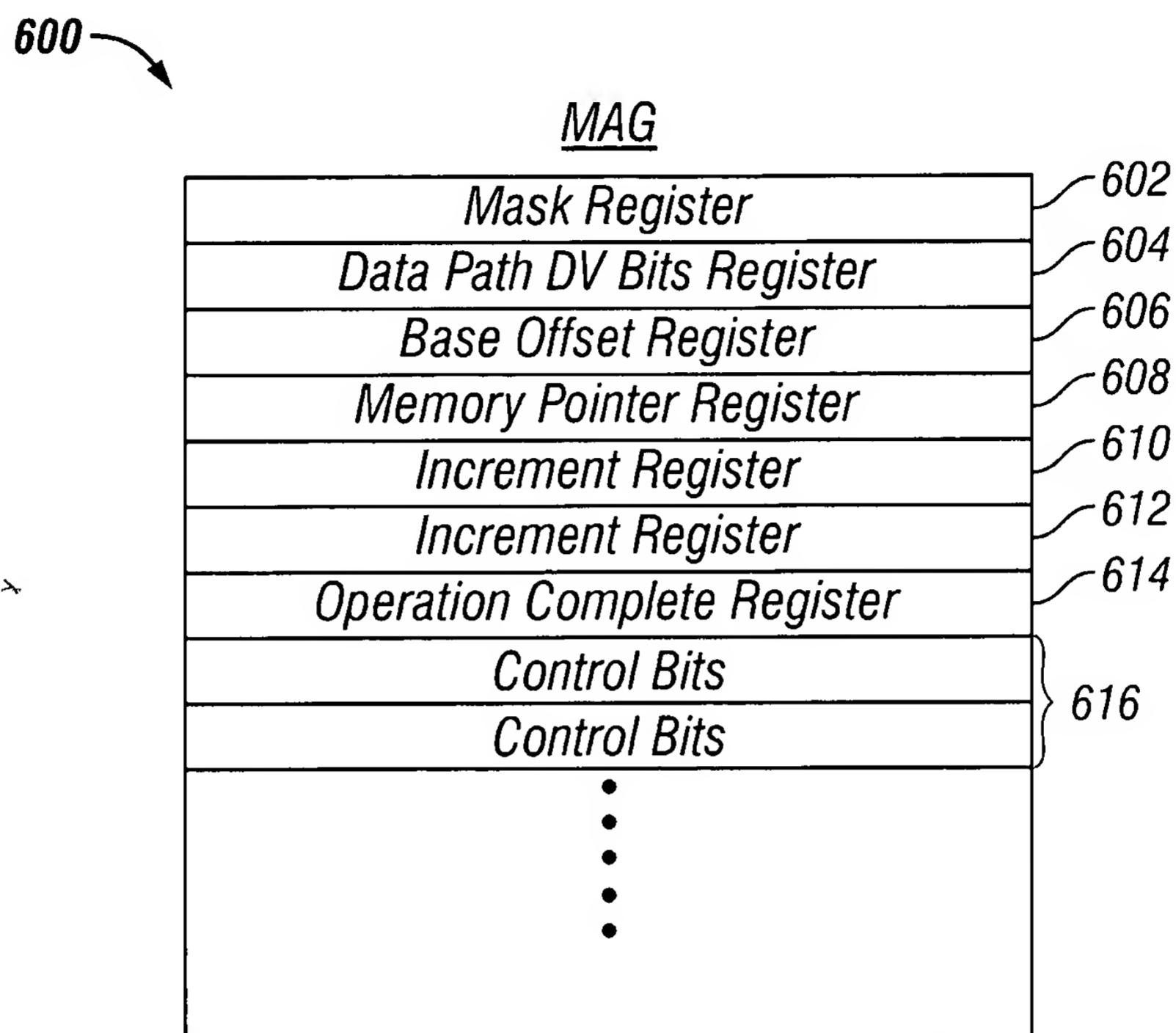


FIG. 6

800

802

15	14	13	12	11	10	9	8-0	
0	0	X	X	X	X	X	X	Read Immediate
1	0	X	X	X	X	X	X	Write Immediate
0	1	0	X	X	X	X	X	Read Indirect
0	1	1	X	X	X	X	X	Write Indirect
1	1	0	1	X	X	X	X	Write Increment Registers
1	1	0	0	0	X	X	X	Set Data Path
1	1	0	0	1	0	0	X	Set Read Operation Complete
1	1	1	0	0	X	X	X	Write Memory Pointer Register
1	1	1	0	1	X	X	X	Write Base Offset
1	1	1	1	0	X	X	X	Write Mask Register
1	1	1	1	1	X	X	X	Write First Use Register

FIG. 8



700 →

MCH Command	Description
702 Write Mask	Used in address calculations to create circular buffer addressing
704 Set Data Path DV Bits	Determines the target PE(s) for the read data
706 Read Immediate	Reads RAM from a specified address
708 Write Immediate	Writes RAM from the Data CCR to a specified RAM address
710 Write MPR	An initial offset value to be used in address calculations
712 Write Increment Register	Provides X and Y increment values for one or 2D addressing
714 Write Base Offset Register	Sets the Base Offset Register used in addressing
716 Read Indirect N Words	Reads N words into the Data CCR using the MAG Memory Pointer
718 Write Indirect N Words	Writes N words from the Data CCR using the MAG Memory Pointer
720 Read OP Complete	Used to signal the MCH control/ PE that a block transfer is complete
722 Infinite Indirect Operation	Set infinite indirect MCH operation

FIG. 7